Optimization of Upstream Memory Read Performance
## Pericom PCI Express Bridge

Introduction

The Pericom PCI Express bridges are used widely in various fields: telecom, surveillance, industrial, and consumer. The PCIe bridge models from Pericom include PI7C9X110, PI7C9X111, PI7C9X112, and PI7C9X130.

Issues in Application

When the PCIe bridge is in forward mode, the PCI or PCIX device initiates upstream memory reads. And because of this, the data transmission efficiency may be low.

This can be observed by initiating upstream memory to read a certain data, and the time consumed in the test can determine the data transmission efficiency.

In addition, the data transmission efficiency is different when MR or MRM is initiated, and the efficiency is also related to the PCI bus frequency (33MHz or 66MHz).
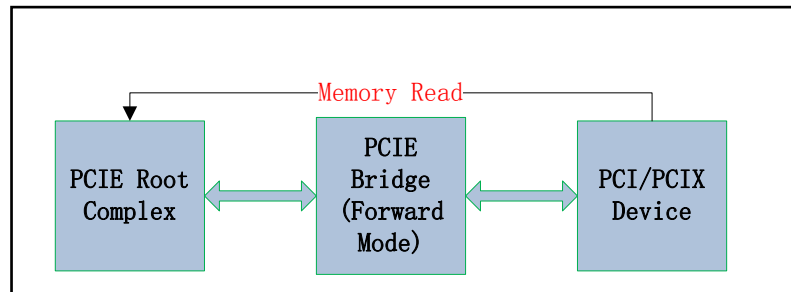
Cause Analysis

The root cause of the transmission efficiency lies in the fact that every time when PCI or PCIX device reads data, it has to wait for the data to be transferred from the root by the bridge.

Because of this, the device is not able to read all the data in the buffer of bridge once. And when the device requests upstream memory read the next time, the PCIE bridge requests data again, and the previous data in the buffer is replaced by the new data. In this way, the abandoned data has never been transferred. And with the time of wait for data, the data transmission efficiency is reduced.

Upstream Memory Read Performance Optimization

According to above analysis, in order to optimize upstream memory read performance, we need to reduce waiting time and read frequency, and fetch data as much as possible. The control registers related to the PCI data buffering are 'Max payload size' and 'Max Read request size'.

Optimization Items

Table 1: PCI data buffering control register, offset 40h

Bit	Function	Description
1	Memory Read Prefetching Dynamic Control Disable	0:enable memory read prefetching dynamic control for PCI to PCIE read 1: disable memory read prefetching dynamic control for PCI to PCIE read
2	Completion Data Prediction Control	0: enable Completion Data Prediction for PCI to PCIE read 1: disable Completion Data Prediction
5:4	PCI Read Multiple Prefetch Mode	00: one cache line prefetch if memory read multiple address is in prefetchable range at the PCI interface 01: full prefetch if address is in prefetchable range at the PCI interface , and PCIE Bridge will keep remaining data after it disconnects the external master during burst read with read multiple command until the discard timer expires 10: full prefetch if address is in prefetchable range at the PCI interface 11: full prefetch if address is in prefetchable range at the PCI interface and PCIE Bridge will keep remaining data after the read multiple is terminated either by an external master or by the PCIE Bridge , until the discard timer expires .
14:12	Maximum Memory Read Byte Count	Maximum Byte Count is used by PCIE Bridge when generating memory read requests on the PCIE link in response to a memory read initiated on the PCI bus and bit[9:8],bit[7:6],and bit[5:4] are set to : "full prefetch " . 000:512 bytes(default) 001:128 bytes 010:256bytes 011:512 bytes 100:1024 bytes 101:2048 bytes 110:4096 bytes 111:512 bytes

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Optimization Result and Conclusion

After setting Control Register Offset 40h bit 1 to "1", and 40h bit[5:4] to "11", 40h bit[14:12] to "110", the data transmission efficiency is improved considerably.

In conclusion, if the data transmission efficiency is very low during PCIe bridge operation when PCI or PCIX device initiates memory read requests, it is recommended to adjust the above optimization items according to the capability of PCI or PCIX device and the quantity of transmission data. The data transmission efficiency can be improved significantly.